



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,683	12/04/2001	Chris E. Barns	10559/584001/P12765	7423

20985 7590 07/25/2003
FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122

EXAMINER

DEO, DUY VU NGUYEN

ART UNIT	PAPER NUMBER
----------	--------------

1765

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/008,683

Applicant(s)

BARNES ET AL.

Examiner

DuyVu n Deo

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 15-22 is/are rejected.
- 7) ☒ Claim(s) 10-14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5-8, 15-17, 20, 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US 6,074,921).

Referring to claim 1, Lin describes a method for fabricating a semiconductor structure comprising: forming silicide regions 41, 51, 33, 35 (claimed silicide layer) over a semiconductor substrate (col. 5, line 17-24), removing silicide regions 41 and 51 (claimed removing a portion of the silicide layer) by chemical mechanical polishing (col. 5, line 50-64).

Referring to claim 15, the method further comprising: forming polysilicon layer members 42, 52 for the gates (claimed polysilicon feature) on a semiconductor substrate (col. 4, line 40, 41), depositing a metallic layer 62 (claimed first metal layer) over the polysilicon feature and reacting the metal layer with the polysilicon feature to form a metal silicide (col. 5, line 12-24); depositing a dielectric layer 70 over the metal layer and the semiconductor substrate (col. 5, line 37-49); removing a portion of the dielectric over metal silicide portions 41 and 51 and removing the portion of the metal silicide by chemical mechanical polishing (col. 5, line 50-64).

Removing of the dielectric layer (also referring to claim 5) must expose the silicide portions 41 and 51 in order to these portions to be removed (figure 1d, 1e).

Application/Control Number: 10/008,683
Art Unit: 1765

Referring to claims 20 and 21, gates 40, 50 that include polysilicon member 42 and 52 are formed by depositing a material over the semiconductor substrate and patterning the material to define a topography having a high and low region where in the high region comprising a polysilicon feature (col. 4, line 36-col. 5, line 10). Forming the metal silicide 41 and 51 on the high region and metal silicide 33, 35 on the low region (col. 5, line 10-24; figure 1b); removing the portion of the metal silicide 41 and 51 on the high region by chemical mechanical polishing (col. 5, line 50-64; figure 1e).

Referring to claim 2, forming gates 40 and 50 that includes polysilicon member 42, 52 would read on claimed high and low regions and they are formed before forming the silicide layer (col. 4, line 36-44). The silicide portions 41 and 51, which are removed, are from the high region (figure 1d, 1e).

Referring to claims 6 and 7, the dielectric layer 70 can be formed from silicon dioxide or silicon nitride (col. 3, line 60; col. 5, line 39-41).

Referring to claims 8 and 16, the portion of the dielectric layer 70 is removed by chemical mechanical polishing (col. 5, line 61-64).

Referring to claim 17, the dielectric layer and the metal silicide must a first and second polishing rate which must be different since they are two different material and the chemical mechanical polishing is preferably suitable for the composition of layer 70 (col. 61-64).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Application/Control Number: 10/008,683
Art Unit: 1765

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3, 9, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

Referring to claim 3, Lin doesn't describe the high region (the gate) is formed by depositing a polysilicon layer and removing a portion of the polysilicon layer. He describes depositing and patterning an amorphous silicon layer and then through RTA to change the amorphous to polysilicon layer (col. 45-col. 5, line 10). Since he teaches that the high region (the gate) would be eventually be a polysilicon layer as shown above and he also teaches that polysilicon is often the material of choice for forming the gates (col. 1, line 10); therefore, it would have been obvious for one skill in the art at the time of the invention to deposit and pattern a polysilicon layer to form a high region (the gate) because polysilicon is the material for forming the gate as described above and a step of changing an amorphous silicon to polysilicon can be omitted which would further simplify the process of forming the gate.

Referring to claim 9, Lin further shows another embodiment wherein a coating 370 (claimed top layer) is formed on a dielectric layer of silicon nitride 368 (col. 9, 17-21). It would have been obvious for one skill in the art to in light Lin's teaching to form a coating 370 (claimed top layer) is formed on a dielectric layer of silicon nitride 368 because he shows that they are an alternative embodiment structure so that a barrier (silicon nitride) and a coating covering the barrier are formed on the trench and connection regions (col. 9, line 17-23).

Referring to claims 18, and 19, Lin further describes in another embodiment where the polysilicon feature is removed to create an opening in the dielectric layer and filling the opening in the dielectric layer with a second metal (col. 9, line 34-42; figure 4c; col. 10, line 1-7; figure 4g). It would have been obvious for one skill in the art to remove the poly and deposit a second

Application/Control Number: 10/008,683

Art Unit: 1765

metal because Lin teaches that the polysilicon member (polysilicon feature) can be partially replaced by metal to provide metal electrode for the gate (col. 1, line 64-col. 2, line 6; col. 10, line 10, 11).

5. Claims 4, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin as applied to claims 3 and 20 above, and further in view of Givens et al. (US 6,080,655).

Referring to claims 4 and 22, Lin doesn't describe the polishing rate of the metal silicide layer is faster than the polishing rate of the polysilicon layer (or material defining the topography). However, Lin describes that the silicide and dielectric layer are polished (or removed) to define a coplanar surface with the polysilicon surface (or material defining the topography) (col. 5, line 50-64). This would suggest that the polysilicon layer is not being polished. Therefore, it would be obvious to one skill in the art to polish the silicide faster than the polysilicon since it is the material that is needed to be removed and not the polysilicon. Furthermore, Givens also teaches that the under layer, which is not being polished, has a lower polishing rate than the upper polished layers so that it acts as an polished-stop layer to endpoints the planarization (col. 6, line 27-57). It would have been obvious for one skill in the art to in light of Givens' teaching to polish the upper silicide faster than the under polysilicon so that the polysilicon can act as a polished-stop layer to endpoints the planarization since Lin teaches that the polishing of the upper silicide and dielectric layer defines a planar surface that is substantially coplanar with the polysilicon surfaces (col. 5, line 55-58).

Art Unit: 1765

Allowable Subject Matter

6. Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-14 are allowable because applied prior art doesn't describe or suggest (claim 10) the top layer comprises a titanium nitride layer. The closest prior art, Lin describes a top layer 370 is an oxide of silicon (col. 9, line 19-21).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 703-305-0515.

DVD
July 22, 2003

